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Source: All Sources: Area of Law - By Topic: Patent Law: Patents: U.S. Patents: Utility Patents

Terms: patno is 5,777,391 (Edit Search)

Pat. No. 5777391, *

5,777,391

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Jul. 7, 1998

Semiconductor device having an improved connection arrangement between a semiconductor pellet and base substrate electrodes and a method of manufacture thereof

REISSUE: Reissue Application filed Jul. 7, 2000 (O.G. Dec. 5, 2000) Ex. Gp.: 2815; Re. S.N.

09/613,541

INVENTOR: Nakamura, Atsushi, Fuchu, Japan

Nishi, Kunihiko, Kokubunji, Japan

ASSIGNEE-AT-ISSUE: Hitachi, Ltd., Tokyo, Japan (03)

APPL-NO: 570,646

FILED: Dec. 11, 1995

FOR-PRIOR:

Dec. 20, 1994 Japan 6-316444 May 25, 1995 Japan 7-126405

INT-CL: [6] H01L 23#49

US-CL: 257#778; 257#777; 257#780; 257#737; 257#784; 438#108; 438#617

CL: 257;438

SEARCH-FLD: 257#780, 777, 778, 737, 738, 697, 784; 438#108, 617

REF-CITED:

U.S. PATENT DOCUMENTS

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OTHER PUBLICATIONS

Nikkei electronics 1994.2.28 (No. 602), pp. 111-117. (with translation).

PRIM-EXMR: Thomas, Tom

ASST-EXMR: Hardy, David B.

LEGAL-REP: Antonelli, Terry, Stout, & Kraus, LLP

CORE TERMS: electrode, bonding, semiconductor, pellet, semiconductor device, electrically, mounting, slit, wire, rigid, substrate, resin, pad, conductor, bump, sealing, connecting, flexible, recess, through-hole, hole, modulus, molding, die, manufacture, thermal, coefficient, row, connect, deformed

ABST:

A semiconductor device comprising a semiconductor pellet mounted on a pellet mounting area of the main surface of a base substrate, in which first electrode pads arranged on the back of the base substrate are electrically connected to bonding pads arranged on the main surface of the semiconductor pellet. The base substrate is formed of a rigid substrate, and its first electrode pads are electrically connected to the second electrode pads arranged on its reverse side. The semiconductor pellet is mounted on the pellet mounting area of the main surface of the base substrate, with its main surface downward, and its bonding pads are connected electrically with the second electrode pads of the base substrate through bonding wires passing through slits formed in the base substrate.

NO-OF-CLAIMS: 25

EXMPL-CLAIM: 1

NO-OF-FIGURES: 16

NO-DRWNG-PP: 13

SUM:

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor device and a method of manufacture thereof and more particularly to a technology effectively applied to a semiconductor device and a method of manufacture thereof, the device having a structure in which a semiconductor pellet is mounted on a pellet mounting area on the main surface of a base substrate and in which a first electrode pad on the back of the base substrate is electrically connected to an external terminal on the main surface of the semiconductor pellet.

A semiconductor device with a ball grid array (BGA) structure has been introduced as a semiconductor device having a high level of integration in the Nikkei Electronics, Feb. 28, 1994, pp. 111-117, published by Nikkei McGraw-Hill. The BGA structure of such as semiconductor device, as shown in FIG. 16 (cross section of an essential part), has a semiconductor pellet 2 mounted on a pellet mounting area of the main surface of the base substrate 1 and a plurality of bump electrodes 4 arranged in grid on the back of the base substrate 1 opposite the main surface.

The base substrate 1 may be made from a printed wiring board of two-layer wiring structure. Second electrode pads 1A are arranged in a peripheral area of the main surface of the base substrate 1 (around the pellet mounting area), while first electrode pads 1B are arranged on the back of the base substrate 1 opposite the main surface. The second electrode pads 1A are electrically connected to through-hole conductors 1C via conductors 1A1 arranged on the main surface of the base substrate 1. The first electrode pads 1B are electrically connected to the through-hole conductors 1C via conductors 1B1 arranged on the back of the base substrate 1.

The semiconductor pellet 2 may comprise mainly a semiconductor substrate 2B of single-crystal silicon. On the main surface of the semiconductor substrate 2B (device forming surface) is formed a logic circuit system, a memory circuit system or a combination of these. A plurality of bonding pads 2A are arranged on the main surface of the semiconductor substrate 2B. The bonding pads 2A are formed in the top of the interconnect layers formed on the main surface of the semiconductor substrate 2B.

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Basic Patent (No, Kind, Date): JP 8227908 A2 19960903
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Patent Family:
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    Patent No
                 A2 19960903
                                 JP 95126405 A
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    JP 8227908
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    US 5777391
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                      19980707
Priority Data (No, Kind, Date):
    JP 95126405 A 19950525
    JP 94316444 A 19941220
PATENT FAMILY:
JAPAN (JP)
  Patent (No, Kind, Date): JP 8227908 A2 19960903
    SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF (English)
    Patent Assignee: HITACHI LTD
    Author (Inventor): NAKAMURA ATSUSHI; NISHI KUNIHIKO
    Priority (No, Kind, Date): JP 95126405 A 19950525; JP 94316444 A
      19941220
    Applic (No, Kind, Date): JP 95126405 A
                                            19950525
    IPC: * H01L-021/60
    Derwent WPI Acc No: * G 96-452755; G 96-452755
    Language of Document: Japanese
UNITED STATES OF AMERICA (US)
  Patent (No, Kind, Date): US 5777391 A
                                         19980707
    SEMICONDUCTOR DEVICE HAVING AN IMPROVED CONNECTION ARRANGEMENT BETWEEN
      A SEMICONDUCTOR PELLET AND BASE SUBSTRATE ELECTRODES AND A METHOD OF
      MANUFACTURE THEREOF (English)
    Patent Assignee: HITACHI LTD
                                  (JP)
    Author (Inventor): NAKAMURA ATSUSHI (JP); NISHI KUNIHIKO (JP)
    Priority (No, Kind, Date): JP 94316444 A 19941220; JP 95126405 A
      19950525
    Applic (No, Kind, Date): US 570646 A
                                          19951211
    National Class: * 257778000; 257777000; 257780000; 257737000;
      257784000; 438108000; 438617000
    IPC: * H01L-023/49
    Derwent WPI Acc No: * G 96-452755
    Language of Document: English
UNITED STATES OF AMERICA (US)
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Legal Status (No, Type, Date, Code, Text):

us 5777391	P	941220 US AA PRIORITY ATENT)
		JP 94316444 A 19941220
บร 5777391	P	19950525 US AA PRIORITY (PATENT)
		JP 95126405 A 19950525
us 5777391	P	19951211 US AE APPLICATION DATA (PATENT)
		(APPL. DATA (PATENT))
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บร 5777391	P	19951211 US AS02 ASSIGNMENT OF ASSIGNOR'S
		INTEREST
		HITACHI, LTD. 6, KANDA SURUGADAI 4-CHOME
		CHIYODA-KU, JAPAN ; NAKAMURA, ATSUSHI :
		19951114; NISHI, KUNIHIKO : 19951114
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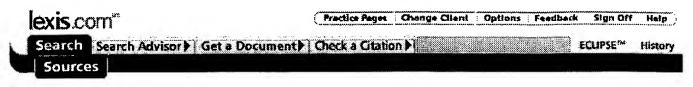
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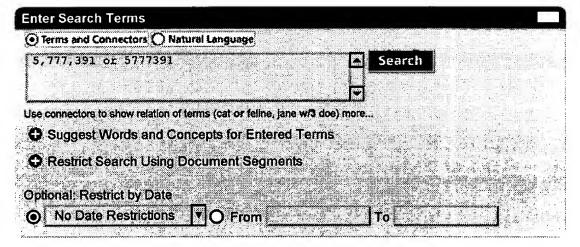
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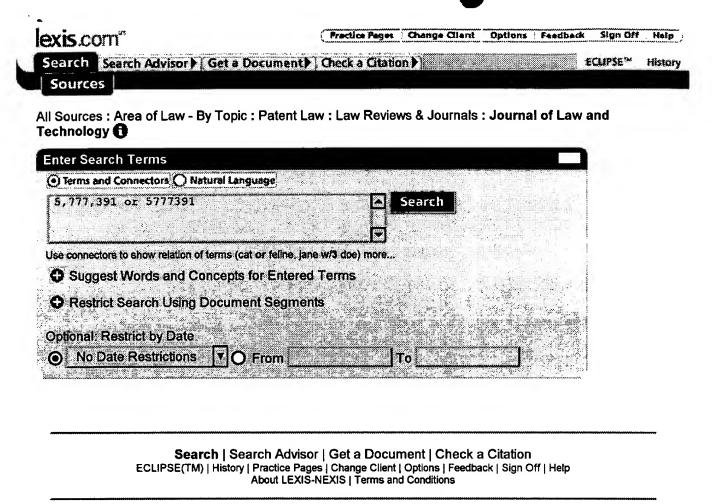
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Search statement 2

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1/1 CRXX - (C) CLAIMS/RRX

AN - 3006688 PN - 5,777,391 A 19980707 [US5777391]

PT - E (Electrical) PA - Hitachi Ltd JP

ACT - 20000707 REISSUE REQUESTED Issue Date of O.G.: 20001205 Reissue Request Number: 09/613541 Examination Group responsible for Reissue process: 2815

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